IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

INVENSAS CORPORATION, **Plaintiff,** **vs.** **SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC.,** **Defendants.**	Civil Action No. 2:17-cv-670 [RWS/RSP] **JURY TRIAL DEMANDED**

DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF

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REGULATIONS

The Samsung defendants hereby submit their Responsive Claim Construction Brief.

I. U.S. PATENT NOS. 6,232,231 (CLAIMS 1-8) AND 6,849,946 (CLAIMS 16-22)

A. "substantially planar / co-planar" ('946, Cl. 16-17; '231, Cl. 1, 4)

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, no construction necessary. Alternatively: Substantially planar: "substantially flat or level"; Substantially co-planar: "substantially at the same elevation"	Indefinite

The parties agree that "substantially planar/co-planar" refer to the degree of flatness of a surface. D.I. 123, 9. The parties also agree that terms of degree are indefinite when the intrinsic record fails to establish "some objective standard for measuring the degree." *Id.*; *see also Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014). Here, the intrinsic record provides no objective standard or boundary to define the degree of flatness that qualifies as "substantially planar/co-planar." The specification, for example, simply repeats the "substantially planar/co-planar" language without further guidance. *E.g.*, '231, 1:8-14 ("This invention relates to integrated circuit manufacturing and, more particularly, to a substantially planarized interconnect topography[.]"). Thus, "substantially planar/co-planar" is indefinite.

Invensas points only to Figure 7 and a single paragraph at (1:28-48) of the specification as purportedly providing criteria. But Figure 7 merely depicts an idealized, perfectly planar surface. It does not provide any guidance as to the degree of acceptable deviation from a perfectly flat surface that would still qualify as "substantially planar/co-planar." *Id.*, 8:13-17. Further, because "patent drawings do not define the precise proportions of the elements," Figure 7 cannot define the metes and bounds of the claim term. *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000).

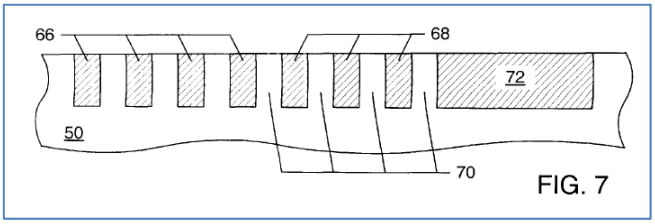


FIG. 7

Invensas argues that the specification provides criteria at 1:28-48 by identifying the objectives of "solv[ing] the problem of elevational disparities" and "provid[ing] a sufficiently flat

surface on which to build the subsequent layers of a semiconductor chip." D.I. 123, 10. It also cites testimony from its expert Dr. Kanicki and inventor Christopher Seams, who defined "substantially planar/co-planar" as "[f]lat enough to pattern subsequent layers."[1] *Id*. (citing D.I. 123-2, ¶¶51-57; D.I. 132-1 at 211:12-212:6). Invensas also cites *Max Blu Technologies, LLC v. Cinedigm Corp.*, No. 2:15-cv-1369-JRG, 2016 WL 3688801 (E.D. Tex. July 12, 2016), and *THX, Ltd. v. Apple Inc.,* No. 13-cv-01161-HSG, 2016 WL 6563340 (N.D. Cal. Nov. 4, 2016), as finding terms with "substantially" definite because the patents tied those terms to design goals.

Invensas's reliance on 1:28-48 as providing an objective standard under *Max Blue*/*THX* is misplaced for two reasons. First, at no point does 1:28-48 indicate when a surface is "substantially planar/co-planar" or describe the patents' goals. '231, 1:28-48. The paragraph only describes problems that could result from "elevational disparities" on a surface. *Id.*; Thomas Decl. ¶46. Moreover, the specification refutes any connection between "substantially planar/co-planar," 1:28-48, and the patents' purported goals. The specification explains that even prior art chemical-mechanical polishing (CMP) could planarize the "surface of the conductive material" to a "level ***substantially*** commensurate with that of the upper surface of the interlevel dielectric." '231, 2:15-18 (emphasis added). It later uses this same "level substantially commensurate" language to describe Figure 7's alleged invention and "substantially planar topography." *Id*., 6:29-35; Thomas Decl. ¶47. Yet it explains that even with a "level substantially commensurate," the "elevational disparities" still exist. *Id*., 2:63-64; Thomas Decl. ¶47. Because both the prior art approach and the alleged invention produce a "substantially planar/co-planar" surface that still suffers from the "elevational disparities" described in 1:28-48, the bounds of "substantially planar/co-planar" cannot be defined by any purported goals of the patents or the text at 1:28-48. Thomas Decl. ¶47.

[1] Mr. Seams also admitted that he had never heard engineers use the terms "substantially planar/co-planar" in practice. Ex. A, 158:16-159:12, 212:7-12. And co-inventor, Anantha Sethuraman, gave a different definition of the terms as "essentially flat." Ex. B, 120:24-121:1, 123:7-11.

Second, the criteria that Invensas offers of "sufficiently flat" or "flat enough" to build subsequent layers fail to provide objective boundaries. Instead, such criteria are subjective and context-dependent. As Dr. Kanicki explains: "the degree of planarity required will vary depending on the tolerances of the particular fabrication process step used during the manufacture of a given chip—including process node, desired feature size, and the depth-of-focus." D.I. 123-2, ¶57. Further, what is "substantially planar" depends on the "design preferences and criteria applicable to any particular chip." *Id.* Similarly, inventor Mr. Sethuraman testified that "[e]very customer has their own way of describing what is needed" for planarity and "[w]ithout knowing the context, I cannot tell you" if a surface is "substantially coplanar." Ex. B, 43:23-44:2, 123:2-11.

Thus, what is "sufficiently flat" or "flat enough" varies widely from one manufacturer, engineer, or chip to the next depending on context and subjective preferences. Thomas Decl. ¶¶51-53. For example, a surface could be "substantially planar" when fabricated with equipment having greater tolerances, a particular process node and feature sizes, but not "substantially planar" when fabricated with equipment having lower tolerances and a different process node and feature sizes. *Id*. And two different engineers having different design preferences could disagree entirely on whether the same surface is "substantially planar." *Id*. The patents fail to provide the necessary context—they do not identify any design preferences, tolerances, process node, or feature sizes. On similar facts in *Icon Health & Fitness, Inc. v. Polar Electro Oy*, the Federal Circuit found terms indefinite when their meanings varied "from person-to-person" and could "have meaning only in the context of a defined reference" that the intrinsic evidence did not identify. 656 F. App'x 1008, 1013-15 (Fed. Cir. 2016). And in *Versata Software, Inc. v. Zoho Corp.*, a court found a term indefinite because its meaning depended on a "user's expectation," was a "moving target," "wholly subjective," and "context-dependent." 213 F. Supp. 3d 829, 837-38 (W.D. Tex. 2016).

Indeed, the lack of guidance in the intrinsic record here makes "substantially planar/co-

planar" comparable to other "substantially" terms that courts have found indefinite. For example, in *Geodynamics, Inc. v. Dynaenergetics US, Inc.*, this Court found "***substantially equal*** to the total depth of penetration" indefinite because neither the specification nor file history provided guidance as to "when the clear tunnel depth is no longer 'substantially equal' to the total depth of the tunnel." No. 2:15-CV-1546-RSP, 2016 WL 6217181, at *15-16 (E.D. Tex. Oct. 25, 2016) (emphasis added). In *Core Wireless Licensing S.A.R.L. v. Apple Inc.*, the court found indefinite claims reciting that a "sender must 'restrict[] the number of consecutive [stolen] frames . . . to a sufficiently low number so as not to ***substantially*** impair the quality of the user information.'" No. 15-cv-05008-PSG, 2016 WL 3124614, at *12 (N.D. Cal. June 3, 2016) (emphasis added). Aside from providing a single example—that one "stolen frame" did not "substantially impair the quality of the user information"—the intrinsic evidence provided no bounds on the number of stolen frames allowed, leaving a "zone of uncertainty—which *Nautilus* bars." *Id*. In *Cayenne Medical, Inc. v. Medshape, Inc.*, the court found "***substantially*** different construction" indefinite because nothing in "the intrinsic evidence . . . would allow one skilled in the art to determine, with reasonable certainty, when the magnitude of change in the 'construction' of the first and second member is no longer insubstantial but rather has become 'substantially' different." No. 2:14-cv-0451-HRH, 2016 WL 2606983, at *6 (D. Ariz. May 6, 2016) (emphasis added).

Because "substantially planar/co-planar" are terms of degree that depend on subjective preferences and contexts that are not resolved by the intrinsic evidence,[2] they are indefinite.

B. "trench" ('946, Cl. 16-17, 20-22; '231, Cl. 1, 3-4)

Plaintiff's Proposal	Defendants' Proposal
"a cavity, or recess, formed in a semiconductor substrate or a dielectric layer"	Plain and ordinary meaning, no construction necessary.

[2] Invensas's last two arguments are irrelevant. First, that the Examiner identified prior art shows neither that it understood the scope of "substantially planar/co-planar," nor that the intrinsic evidence provides objective bounds. Likewise, that three Samsung patents use "substantially planar" is irrelevant to whether the intrinsic evidence for these patents provide objective bounds.

"Trench" is a lay term that has a well-understood meaning that the jury can apply without construction. *See, e.g.*, Ex. C, 1907 ("A deep furrow or ditch"). The claims do not use "trench" in a different or special manner. Thomas Decl. ¶57. Nonetheless, Invensas argues for a construction to preclude Samsung from relying on the "shape of trenches" to argue non-infringement, and it cites an ITC ALJ's decision in another matter in support. D.I. 123, 11-13. Yet its own construction is silent on the issue of "shape" and thus does nothing to advance its argument. Moreover, Invensas omits that the Commission ordered review of the ALJ's interpretation. *Certain Semiconductor Devices*, 337-TA-1010, 2017 WL 6434980, at *3-4 (USITC Sept. 29, 2017); 19 CFR §210.43(b)(ii). The matter settled before a final determination.

Invensas's proposal, meanwhile, improperly injects limitations not found in the intrinsic record. Instead, Invensas relies on a construction of "trench" from another case, *STMicroelectronics v. Broadcom*, No. 4:02-cv-00362-RAS, D.I. 156 at 126-32 (E.D. Tex. Jan. 2, 2004). *STMicroelectronics*, however, construed "trench" in an unrelated patent directed to "shallow trenches" and followed that patent's language of "semiconductor substrate 22 or wafer having relatively shallow trenches 15, cavities, or recesses." Ex. D, 5:2-5; Thomas Decl. ¶¶59-60.

That construction is inapplicable to the '231 and '946 Patents. The construction's language of "a cavity, or recess" implies shallower areas than a "trench." The patents do not describe trenches as "shallow," and the word "cavity" is never used in the intrinsic record. "Recess" appears in the specification, but only to describe shallow surface deformations called "recessed areas" 40 and 42 that, as annotated in blue in Figure 4, are distinct from the deeper "trenches" in which interconnects 36 and 38 are formed. '231, 2:63-67. Further, the construction's reference to trenches in a "semiconductor substrate" contradicts the claims' recitation of forming "trenches [in/into] a ***dielectric layer.***" '946, Claim 16; '231, Claim 1. The specification similarly describes forming

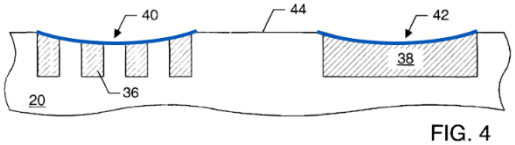


FIG. 4

"trenches" in the "dielectric layer." *E.g.*, '231, 6:53-7:6. The specification's only two mentions of "semiconductor substrate" include no suggestion of forming trenches in it. *Id*., 1:15-25, 3:64-4:11. Invensas's proposal therefore should be rejected as inconsistent with the intrinsic record.

C. "dummy conductors" ('946, Cl. 16-18; '231, Cl. 1, 4)

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, no construction necessary. Alternatively: "conductive structures that are not connected to any active or passive devices that function as an integrated circuit"	"conductive structures that can carry power or ground voltages but are not connected to any active or passive devices that function as an integrated circuit"

While asserting that the common word "trench" has "specialized meaning," Invensas inexplicably argues that "dummy conductors" does not require construction although it is a defined term in the patents with specialized meaning in the context of fabricating interconnects. The specification defines "dummy conductors" in two passages, excerpted below. Samsung's proposal follows verbatim from these definitions, which specify the capability of carrying power or ground:

- "Dummy conductors 68 are not connected to any active or passive device which forms an integrated circuit of the semiconductor topography shown in FIG. 7. While ***dummy conductors can carry power or ground voltages***, they do not carry transitory voltages or current associated with an operable circuit." '231, 8:4-9 (emphasis added).

- "The dummy conductors are electrically separate from electrically conductive features of the ensuing integrated circuit . . . The dummy conductors therefore do not contain transitory voltages and/or current associated with or connected to active and passive devices within the semiconductor topography. Most likely, the ***dummy conductors are connected to a power supply or ground*** . . . ." *Id*., 4:35-44 (emphasis added).

Invensas mischaracterizes the capability of carrying power or ground as optional. D.I. 123, 13-14. The passages above define the characteristics of "dummy conductors" as a whole. *See Trs. of Columbia Univ. v. Symantec Corp.*, 811 F.3d 1359, 1365 (Fed. Cir. 2016) (finding two statements describing characteristics of "byte sequence feature" were "not simply descriptions of the preferred embodiment but are statements defining" the term). While Invensas accepts the "not connected to any active or passive devices . . ." requirement of these definitions, it omits the "can

carry power or ground voltages" requirement, making its proposal incomplete. *See Hospira, Inc. v. Fresenius Kabi USA, LLC*, No. 16 C 651, 2017 WL 5891058, at *5 (N.D. Ill. Nov. 27, 2017) (rejecting construction that "relie[d] on an incomplete quotation of the patent's definition and cuts out" other aspects of the definition). Although the second passage hedges by including "[m]ost likely," the specification does not disclose a contrary embodiment where the "dummy conductors" are not connected to power or ground. And as both parties' experts aver, having "dummy conductors" carry power or ground is advantageous because it reduces noise between interconnects and also ensures that "dummy conductors" "do not carry transitory voltages or current"—another defining characteristic of the term. D.I. 123-2, ¶78; Thomas Decl. ¶71; '231, 8:4-9. [3]

Invensas argues that Figure 7 does not show "dummy conductors" with ground or power connections. But as Invensas's expert concedes, Figure 7 is only a "partial cross-sectional view" "that do[es] not reveal the full extent of the dummy trenches" and conductors. D.I. 123-2, ¶78 (citing '231, 6:18-35); *see also* Thomas Decl. ¶69. Thus, Samsung's construction does not exclude any embodiment but instead fully captures the definition of "dummy conductors."

D. "conductive lines" ('946, Cl. 16, 19)

Plaintiff's Proposal	**Defendants' Proposal**
Plain and ordinary meaning, no construction necessary. Alternatively: "a line of conductive material"	"conductive structures that are connected to one or more active or passive devices that function as an integrated circuit"

Construction of "conductive lines" is necessary to distinguish them from "dummy conductors" (the prior term) and to prevent jury confusion as to whether the two terms are overlapping in scope. In contrast to the "dummy conductors," which the parties agree are "***not*** connected to any active or passive devices," the "conductive lines" "***are*** connected to one or more

[3] Invensas's accusation that Samsung is attempting to "confuse" the jury and use "sleight of hand" (D.I. 123, 13-14) is entirely baseless. Samsung's proposal follows verbatim from specification passages that Invensas characterizes as "clear" in meaning. *Id*., 14.

active or passive devices." Invensas's proposals, however, leave ambiguous whether "conductive lines" connect to devices and thus permit the term to encompass "dummy conductors," despite the clear distinctions that the claims and specification draw between the two.

Claim 16 recites an arrangement having two types of conductive structures: (1) "dummy conductors" formed in "dummy trenches" located "between a first trench and a series of second trenches," and (2) "conductive lines" formed in "said series of second trenches and said first trench." Claim 16's arrangement is depicted in Figure 7 below and described repeatedly in the specification. But the specification never uses the claim term "conductive lines." It instead uses the word "interconnect" at least 75 times to refer to the conductive structures formed in the trenches on the two sides of the "dummy conductors." Referencing Figure 7, the specification describes "narrow interconnect[s] 66 [green] . . . formed exclusively in trenches 52, dummy conductors 68 [gray] . . . formed in dummy trenches 56, and a relatively wide interconnect 72 [red] . . . formed in trench 54." '231, 7:40-48. Thus, the "interconnects" in the specification correspond to the "conductive lines" in Claim 16. *See GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1370-71 (Fed. Cir. 2016) (construing "node" as "pager" because the specification "repeatedly and exclusively" used "pager" "over 200 times . . . to refer to the devices in the patented system"); Thomas Decl. ¶80. Because the "conductive lines" are synonymous with "interconnects," they must be connected to devices of an integrated circuit. As the specification explains, the "***interconnect***" is "***connected*** to the implant regions and/or the gate areas" and the "interlevel dielectric and interconnect . . . ***form a multi-level integrated circuit.***" '231, 1:21-27 (emphasis added). By contrast, the "dummy conductors" are "***not*** connected to any active or passive device which forms an integrated circuit." *Id.*, 8:4-7 (emphasis added).

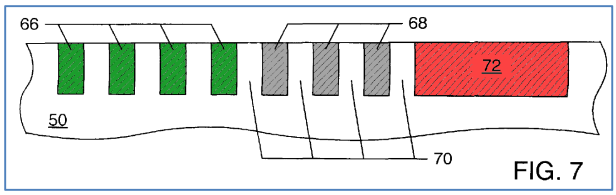
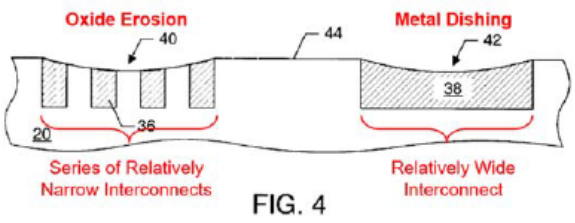
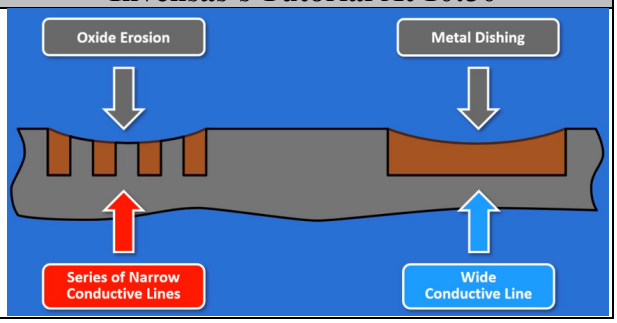


FIG. 7

Invensas agrees that "interconnects" are connected to devices. D.I. 123, 3. It argues,

however, that "conductive lines" are not "interconnects" simply because they are different phrases. *Id*., 16. Invensas's argument is contradicted by the specification described above, which its brief never addresses. It is also contradicted by its own expert declaration, which states that "in the '231 and '946 patents, '***dummy conductors***' are the conductive structures that are inserted between the narrow and wide ***interconnects (or conductive lines)***." D.I. 123-2, ¶63 (emphasis added). This testimony fully supports Samsung's construction by equating "conductive lines" with "interconnect," while also distinguishing "conductive lines" from "dummy conductors." Moreover, Invensas's tutorial and brief label the same elements 36 and 38 in Figure 4 below as "interconnects" and "conductive lines," thereby acknowledging the two terms as synonymous.

Invensas's brief (D.I. 123) At Page 4	**Invensas's Tutorial At 10:30**
 FIG. 4	

Invensas further contends that "conductive lines" and "interconnect" have different meanings because the applicant amended Claim 16 (original claim 17) during prosecution to replace "interconnect" with "conductive lines." D.I. 123, 16. But Invensas fails to note that after this amendment, the applicant equated the two terms when it distinguished prior art from all Claims 1-22 on grounds that none disclosed "form[ing] dummy conductors between a relatively wide ***interconnect*** feature and a series [of] relatively narrow ***interconnect***." Ex. E ('946 FH) at INV-SAM-8667 (emphasis added). The applicant's persistent use of "interconnect" in reference to all claims, including Claim 16 that uses the alternative phrase "conductive lines," confirms the interchangeability of the two terms. *See Single Touch Interactive, Inc. v. Zoove Corp.*, No. 12–cv–831 YGR, 2013 WL 3802805, at *5 (N.D. Cal. July 17, 2013) (finding "access code" and

"specialized access code" interchangeable where the amended claims referred to "specialized access code," but the applicant's remarks referred to them as "access code").

Because "conductive lines" have connections to devices while "dummy conductors" do not, construction of both terms is needed to distinguish the two terms and avoid jury confusion. Accordingly, Samsung proposes that "conductive lines" "***are*** connected" to devices, while "dummy conductors" "are ***not*** connected." Invensas's proposals of no construction or "a line of conductive material," on the other hand, fail to distinguish "conductive lines" from "dummy conductors." Under its proposals, "conductive lines" need not be connected to devices and could encompass "dummy conductors." But the intrinsic evidence does not provide any basis for finding that a "dummy conductor" can be a "conductive line." Moreover, construing "conductive lines" to encompass "dummy conductors" would allow Claim 16 to encompass an arrangement devoid of any interconnect, which defies the patents' objective of planarizing interconnects. *Asyst Techs., Inc. v. Emtrak, Inc.*, 402 F.3d 1188, 1194 (Fed. Cir. 2005) (rejecting construction that "is in tension with one of the objectives . . . expressed in the specification"). The patents' title is "***Planarized semiconductor interconnect topography*** and method for polishing a metal layer to form ***interconnect***," and the specification states the "invention relates . . . to a ***substantially planarized interconnect topography***." '231, 1:8-14 (emphasis added). Invensas itself characterizes the claimed invention as improving planarity "where a series of relatively narrow ***interconnects*** is spaced from a relatively wide ***interconnect.***" D.I. 123, 4 (emphasis added). Because Invensas's proposal contravenes a "fundamental feature of the invention," it should be rejected. *Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1324 (Fed. Cir. 2008).

E. "plurality of laterally spaced dummy trenches" ('946, Cl. 16; '231, Cl. 1)

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, no construction necessary. Alternatively: "two or more dummy trenches arranged with spaces between their sides"	"two or more separate dummy trenches arranged with spaces between their sides"

Invensas mischaracterizes the parties' dispute in asserting that it "seeks the plain and ordinary meaning" whereas Samsung "seeks to add the redundant and confusing limitation that dummy trenches must also be 'separate.'" D.I. 123, 16. To the contrary, Samsung proposes "separate" to give meaning to "plurality," as a "plurality" necessarily refers to more than one "dummy trench" structure. Invensas, meanwhile, seeks to eviscerate "plurality" from the claims by allowing "plurality" to cover a single structure comprising interconnected "dummy trenches."

The specification is consistent with Samsung's view that "plurality of . . . dummy trenches" refers to separate "dummy trench" structures. All embodiments, including those in Figures 5-7, show the "plurality of dummy trenches" as physically separated, not connected. '231, 7:4-11. None show them as a single interconnected structure. Further, past cases construing "plurality" terms have adopted a "separate" requirement. *E.g.*, *Stragent LLC v. Intel Corp.*, No. 6:11-cv-421, 2014 WL 4262451, at *1-2 (E.D. Tex. Apr. 7, 2014) (construing "***plurality*** of CRC circuits" to mean "***separate*** circuits that do not share an output register or feedback paths" (emphasis added)).

In opposing the "separate" requirement, Invensas makes contradictory arguments. While it asserts that the "dummy conductors connected to common power or ground would typically be ***connected to each other***, and thus are not separate," it also emphasizes that the "dummy conductors must be '***electrically separate***'" according to the specification. D.I. 123, 17 (emphasis added). Invensas also errs in asserting that connections between "dummy conductors" and a "common power or ground would" be formed by connecting the laterally spaced "dummy conductors" and "dummy trenches" "to each other." *Id*. Such a possibility is never disclosed in the intrinsic record and would impair planarization, increase manufacturing cost, and reduce design flexibility. Thomas Decl. ¶89. Instead, any connections between "dummy conductors" and a common ground or power supply would be formed through vias in the dielectric layers. *Id*. Thus, Invensas's attempt to read "plurality" out of the claim should be rejected.

II. U.S. PATENT NO. 6,054,336 (CLAIMS 1-2)

A. "forming a conductor pattern on the conductive layer" (Cl. 1)

Plaintiff's Proposal	Defendants' Proposal
"forming a pattern to be transferred to the conductive layer"	"forming a pattern in the conductive layer with gaps corresponding to the auxiliary windows"

The parties have two disputes with this term. First is whether the "conductor pattern" is formed "***in*** the conductive layer" (as Samsung proposes) or formed in a dielectric layer for later "***transfer[] to*** the conductive layer" (as Invensas proposes). *See* D.I. 123, 19. Second is whether the form of the "pattern" has "gaps corresponding to the auxiliary windows" (as Samsung proposes) or whether the form of the "pattern" is unbounded (as Invensas proposes).

1. "conductor pattern" is a "pattern in the conductive layer"

Invensas disregards the plain meaning of "***conductor*** pattern" by arguing that it is not a "pattern in the conductive layer." It instead tries to leverage an ambiguity in the term "conductor pattern ***on*** the conductive layer" to argue that the "conductor pattern" is formed in the "first dielectric layer" that is on top of or "above" the "conductive layer." D.I. 123, 18-19. The intrinsic evidence refutes Invensas's interpretation. The specification uses "conductor pattern" twice, and both instances support Samsung's construction. Fair Decl. ¶51. The summary of the invention states that "[a]ccording to the ***invention . . . the conductor pattern is formed <u>in</u> the conductive layer***." '336, 2:2-11 (emphasis added). The specification also explains that the "conductor pattern" is formed "from" the "conductive layer," which necessarily means that the resulting pattern is formed in the "conductive layer": "[t]he ***invention*** relates to a method of manufacturing an electronic device whereby a ***conductive layer*** is provided on an electrically insulating substrate, ***from which layer a conductor pattern is formed***." *Id*., 1:5-9 (emphasis added). Courts routinely construe claims to be consistent with such statements about the "invention." *E.g.*, *Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318 (Fed. Cir. 2006). Indeed, the specification never

refers to a "conductor pattern" formed in a layer other than the conductive layer.

Nothing Invensas cites leads to a different conclusion. Invensas relies on original Claim 1's limitation, "whereby a conductive layer is provided on an electrically insulating substrate, from which layer a conductor pattern is formed by means of a mask comprising a dielectric layer in which said pattern is defined." D.I. 128-1, INV-SAM-00000555 (underline added). But Invensas tellingly omits the underlined language, which demonstrates that, while a "pattern" can be defined in the "dielectric layer," the "***conductor*** pattern" must be formed from the "conductive layer." Invensas also cites dependent Claim 5, which recites "the conductor pattern is formed ***in*** the conductive layer." Invensas argues that this "distinguish[es]" where the "conductor pattern" is formed in Claim 1 versus the "conductor pattern" of Claim 1 because "[w]hile claim 1 refers to the conductor pattern 'on' the conductive layer, claim 5 refers to the conductor pattern 'formed in the conductive layer.'" D.I. 123, 18. Invensas's argument fails because "***the conductor pattern***" in dependent Claim 5 finds antecedent basis in Claim 1's "a conductor pattern." Thus, Claim 5's "conductor pattern" must be the same as or a subset of Claim 1's "conductor pattern" — it cannot refer to an entirely different "conductor pattern" formed in another layer. Fair Decl. ¶¶52-54.

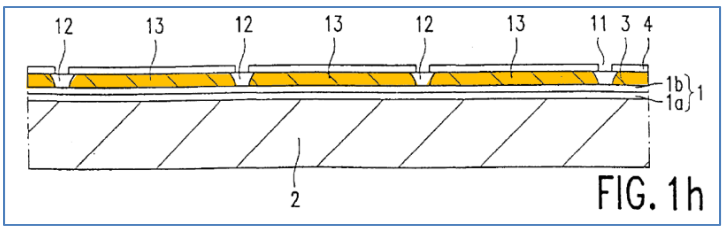
Finally, the "to be transferred" language in Invensas's proposal improperly adds a future, unrecited step of transferring a pattern to the conductive layer. In *SiRF Technology, Inc. v. International Trade Commission*, the Federal Circuit rejected a similar proposal to construe a "communicating" step to require unrecited steps of "forwarding" and "downloading," even when these unrecited steps were implicit in "communicating." 601 F.3d 1319, 1330 (Fed. Cir. 2010). Thus, "conductor pattern" should be construed to mean a "pattern ***in*** the conductive layer."

2. The "pattern" has "gaps corresponding to the auxiliary windows"

Invensas scarcely addresses the second dispute concerning whether the recited "pattern" must have "gaps corresponding to the auxiliary windows." The '336 Patent repeatedly emphasizes

that the conductor "pattern" must be formed with gaps corresponding to the "auxiliary windows" in order to achieve the patent's object of making these gaps narrower than what prior art lithography could achieve. *E.g.*, '336, Abstract. The Federal Circuit has consistently construed claims in a manner that "achieve[s] the overall object of the invention," while rejecting constructions "in tension with . . . the objectives of the [patent] as expressed in the specification and the prosecution history." *Praxair*, 543 F.3d at 1324; *Asyst*, 402 F.3d at 1194. In *Praxair*, the Federal Circuit construed "flow restrictor" as "a structure that serves to restrict the rate of flow sufficiently to prevent a hazardous situation" because the "[t]he fundamental object of the invention . . . is to prevent a hazardous situation from the uncontrolled discharge of gas." 543 F.3d at 1324. In *Asyst*, because the patent's object was a "distributed processing system" that "does not require centralized control," the Federal Circuit rejected plaintiff's broad construction that would allow for "a system [that] would no longer feature localized control, but would be centralized in nature." 402 F.3d at 1194-95. And in *Technology Patents LLC v. T-Mobile (UK) Ltd.*, the Federal Circuit construed "initiates paging operations in another country in a predetermined order" as requiring "creat[ion] by the receiving user." 700 F.3d 482, 493 (Fed. Cir. 2012). The court rejected plaintiff's argument that "the order need not be determined by the receiving user," because it "ignores a substantial amount of intrinsic evidence and the very purpose of the claimed invention . . . [of] allow[ing] users to be paged only in countries that they selected." *Id.*

Here, the '336 Patent's object is to form gaps in a conductive layer that are narrower than what could be formed using prior art lithography, resulting in a "conductor pattern" of conductor "gates" or "electrodes" separated by these gaps. Fair Decl. ¶57. For example, the Abstract states: "The invention renders it possible to make very small inter-electrode gaps in a single conductor layer." '336,



Abstract. The background states: "The invention accordingly has for its further object to provide . . . very narrow gaps between the conductor tracks." *Id.*, 1:64-67. The detailed description states the "invention . . . may be applied wherever electrodes are to be provided at very small distances from one another." *Id.*, 3:3-18. Figure 1h depicts a conductor pattern as "gates" 13 (orange) separated by narrow gaps 12. *Id.*, 4:15-19.

In every embodiment, the narrow gaps are formed using "auxiliary windows," which serve as funnels for etching progressively narrower windows and gaps. Figure 1b below depicts using lithography to form the "auxiliary windows" 8 (circled in pink) in dielectric layer 4, 5 (blue) located above a conductive layer 3 (orange) and substrate 2 (green). *Id.*, 3:45-58. Then, in Figure 1d below, "spacers" 10 (yellow) are formed "on the side walls of the auxiliary windows 8," which "strongly reduc[es] the dimensions of the auxiliary windows 8." *Id.*, 3:62-4:1; Fair Decl. ¶¶59-60.

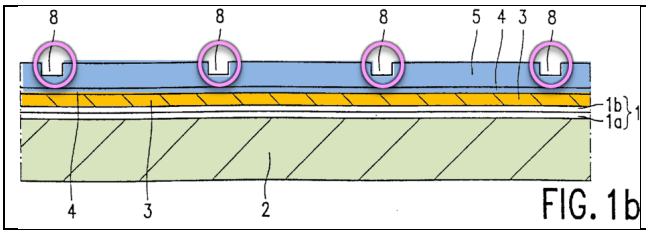


FIG. 1b

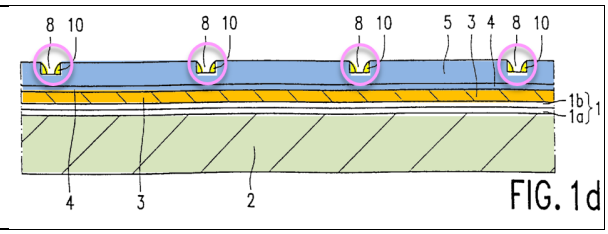


FIG. 1d

The auxiliary windows, as narrowed by the spacers, are then etched until narrower "windows 11" (circled in red) at the conductive layer 3 are formed above the conductive layer as shown in Figure 1f below. '336, Figs. 1c-1f, 3:59-4:11. Then, areas of the conductive layer beneath the windows 11 are oxidized. *Id.*, 4:11-19. This results in a conductor pattern with "gates 13" (orange) separated by gaps 12. *Id.* Notably, these gaps 12 are formed only in areas where the auxiliary windows 8 were formed beforehand. Fair Decl. ¶¶61-62. The specification emphasizes that by forming the gaps using the auxiliary windows 8, the gaps are necessarily smaller than the auxiliary windows 8. *E.g.*, '336, 3:54-58 ("windows 8 in the oxide layer 5 have dimensions . . . considerably greater . . . than those of the gaps to be formed in the conductive layer 3").

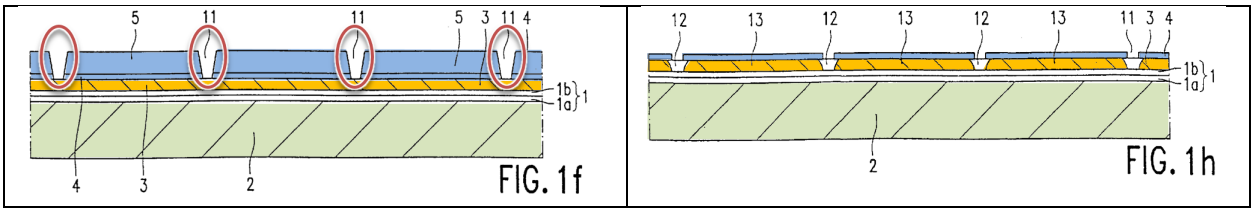


FIG. 1f FIG. 1h

Claim 1 recites each of the above steps and layers, including: a "substrate"; a "conductive layer"; a "dielectric layer"; "forming auxiliary windows in the first dielectric layer"; "form[ing] spacers on the sidewalls of the auxiliary windows"; and etching "through the auxiliary window and the spacers to define the windows at the conductive layer." Claim 1 also recites that the gaps in the conductive layer are smaller than the auxiliary windows, stating "auxiliary windows . . . are greater, in at least one dimension, than the windows to be formed at the conductor layer."

During prosecution, the applicant emphasized that these steps, including the use of "auxiliary windows," are required to enable the formation of narrow gaps or "windows":

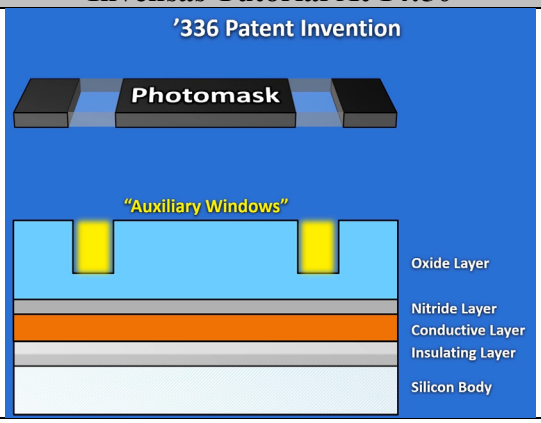
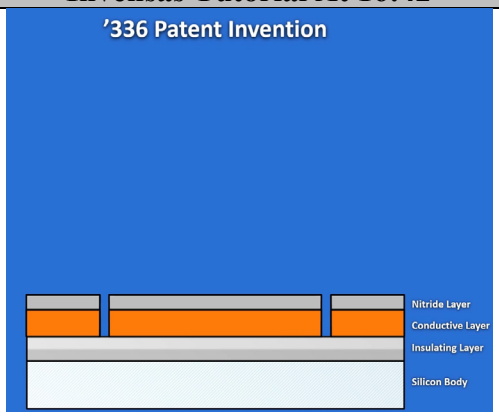
> A particularly relevant feature of the present invention is a formation of auxiliary windows 8 in a first dielectric layer, followed by the addition of a second layer 9, and the anisotropic etching of this second layer 9 to form the spacers 10, followed by further etching. This combination of steps provides a ***window 11 at the conductive layer 3 which is narrower than the auxiliary window 8*** initially formed, shown in Fig. 1b. This facilitates the formation of very narrow conductor tracks.

Ex. F ('336 FH) at INV-SAM-753-54 (emphasis added). The applicant relied on these steps and features to distinguish prior art, arguing "neither Hsu nor Meyyappan [i.e., prior art] . . . define a window at the conductive layer which is smaller in at least one direction on the auxiliary window initially formed in the first dielectric layer." *Id*.

In light of the intrinsic record, including the '336 Patent's stated object and corresponding method, Samsung proposes that the "pattern" must have "gaps ***corresponding*** to the auxiliary windows." This proposal follows from the intrinsic record's disclosure that the gaps can only be formed in places corresponding to where the auxiliary windows were formed previously. In this way, the patent achieves its object of ensuring that these gaps are smaller than the "auxiliary

windows" formed using lithography. Fair Decl. ¶66.

Although Invensas rejects Samsung's construction, its brief and technology tutorial are consistent with Samsung's position. Its brief explains that in the '336 Patent, "[auxiliary] windows are made in the incipient mask using conventional photolithography," "[t]he windows are then narrowed by creating sidewall spacers resulting in smaller windows," and then "[t]he smaller windows create a conductor pattern." D.I. 123, 6. Using this method enables "smaller patterns than possible with ordinary photolithography." *Id*. Its tutorial below also depicts the '336 Patent's process of first forming two auxiliary windows using lithography, and later forming two narrower gaps in places corresponding to where the auxiliary windows were before.

Invensas Tutorial At 14:50	Invensas Tutorial At 16:42
	

Despite acknowledging the correspondence between the gaps of the "conductor pattern" and the "auxiliary windows," Invensas's proposal dissociates the two and leaves the form of the "pattern" ambiguous so that it could include gaps outside of the auxiliary windows. The '336 Patent, however, does not contemplate forming gaps anywhere but within the auxiliary windows. *See Profectus Tech. LLC v. Huawei Techs. Co.*, 823 F.3d 1375, 1381 (Fed. Cir. 2016) (construing claims to require "mounting feature" because plaintiff "fails to pinpoint in the intrinsic record where the patent contemplates a situation where no mounting features exist"). If the gaps were formed outside the auxiliary windows, then those gaps would be formed using lithography in the same conventional way as the "auxiliary windows." Fair Decl. ¶67. As a result, the gaps would

be as wide as the auxiliary windows, rather than narrower as the patent requires. *Id*. Because the requirement of "gaps corresponding to the auxiliary windows" is necessary to achieve the patent's object of gaps narrower than the auxiliary windows, Samsung's construction should be adopted.

B. "continuing etching anisotropically through the auxiliary window and the spacers to define the windows at the conductive layer" (Cl. 1)

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, no construction necessary.	"without interruption, to go on etching anisotropically the first dielectric layer to define windows at the conductive layer only within the auxiliary window"[4]

The disputed term, "continuing etching . . .," is the final step in Claim 1 and follows the step of "etching the additional dielectric layer. . . ." The parties have two disputes. First is where the "windows at the conductive layer" can be formed: Samsung proposes that the "windows at the conductive layer" must be formed "only within the auxiliary window" consistent with the intrinsic evidence, while Invensas proposes no limitation. Second is whether there can be an interruption between the time when the "continuing etching" step begins and the prior "etching" step ends.

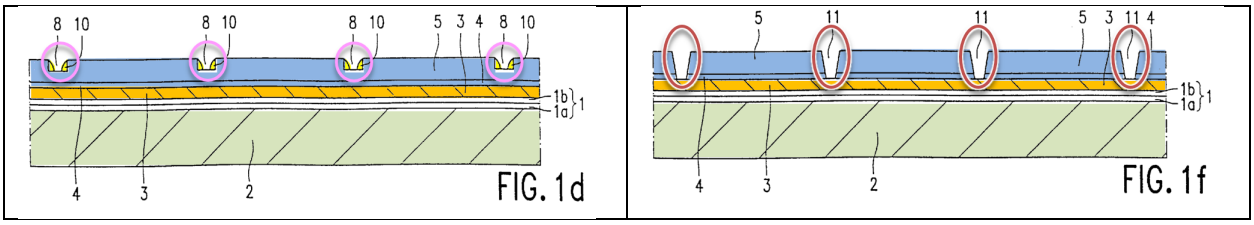
1. Each "window at the conductive layer" is formed and located only within a corresponding "auxiliary window"

The claim term itself recites that the "windows at the conductive layer" are defined "through the ***auxiliary window***" consistent with Samsung's construction. Invensas argues that Claim 1 more broadly encompasses forming "windows at the conductive layer" outside of the "auxiliary window." D.I. 123, 21. But the specification's emphasis on the claimed invention's object of forming gaps narrower than what prior art lithography could achieve precludes Invensas's broad construction. *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1370 (Fed. Cir. 2003) (holding "where the specification makes clear . . . that the claimed invention is narrower that the

[4] Samsung has revised its proposed construction to clarify the parties' dispute and address Invensas's objections to Samsung's prior proposal on grounds that "continuing etching" can occur outside of the auxiliary windows and that "windows at the conductive layer" should not be omitted from the construction. D.I. 123, 21-22.

claim language might imply, it is entirely permissible and proper to limit the claims"). The patent achieves this object by forming "auxiliary windows" using lithography and then using the "auxiliary windows" as funnels for etching narrower windows. The disputed "continuing etching . . ." term is one step in this process that produces narrower "windows at the conductive layer."

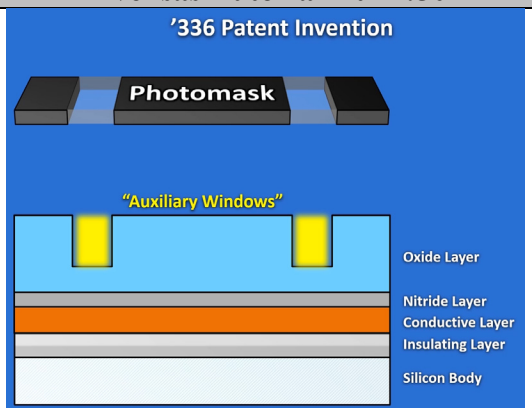
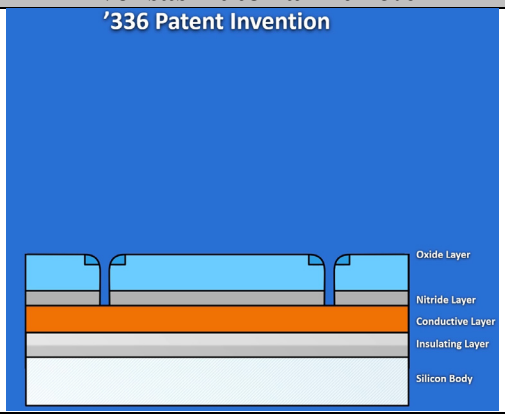
The specification discloses only a single embodiment for the step of "continuing etching" to define "windows at the conductive layer," depicted in Figures 1d and 1f below. Figure 1d shows four auxiliary windows 8 (circled in pink) narrowed by spacers 10 (yellow) formed in a dielectric layer 4, 5 (blue) located above a conductive layer 3 (orange). '336, 3:27-44, 3:59-4:1. Figure 1f shows that after continued etching of the dielectric layer, four windows 11 (circled in red) at the conductive layer 3 are formed. *Id.*, 4:1-11. These windows are the "windows at the conductive layer" recited in the disputed term. Fair Decl. ¶73. And these "[w]indows 11 . . . are substantially smaller than the dimensions of the original [auxiliary] windows 8." '336, Abstract.



Thus, in the patent's sole embodiment of the "continuing etching" step, there is a direct correspondence between the four narrow "windows at the conductive layer" (in Figure 1f) and the four wider "auxiliary windows" (in Figure 1d). Each "window at the conductive layer" is defined by continued etching within a corresponding "auxiliary window." Fair Decl. ¶74. Samsung therefore proposes that the continued etching defines "windows at the conductive layer only within the auxiliary window." This construction recognizes that the "windows at the conductive layer" are defined and located only in areas within the auxiliary windows formed earlier.

Invensas does not dispute the correspondence between the "windows at the conductive layer" and the "auxiliary windows." Indeed, its brief explains that after "[auxiliary] windows are

made in the incipient mask using conventional photolithography," these "windows are then narrowed by creating sidewall spacers resulting in smaller windows" at the conductive layer. D.I. 123, 6. Its technology tutorial confirms the correspondence, with the left figure showing two auxiliary windows formed using lithography and the right figure showing two narrower "windows at the conductive layer" later formed entirely within the two auxiliary windows.

Invensas Tutorial At 14:50	Invensas Tutorial At 16:07
	

Invensas nonetheless argues that the claim's "open-ended language" suggests "other possibilities are allowed." D.I. 123, 23. But Invensas never describes these "other possibilities." Nor could it. The patent never discloses or enables forming "windows at the conductive layer" outside of the auxiliary windows formed earlier. Doing so, as Invensas's proposal allows, would mean that the "windows at the conductive layer" are not formed by etching within auxiliary windows narrowed by spacers, but instead using lithography. Fair Decl. ¶¶75-77. As a result, these windows would be the same width as the auxiliary windows formed earlier using lithography. *Id*. But this would fail to achieve the patent's object of forming "windows at the conductive layer" that are narrower than the "auxiliary windows." *Id*.; '336, Abstract. It would also defy the patent's method to meet this object, which defines "windows at the conductive layer" only within the "auxiliary windows." '336, 3:45-4:11. The applicant relied on these features to distinguish prior art, explaining that Claim 1's "combination of steps" "provides a window 11 at the conductive layer 3 which is narrower than the auxiliary window 8 initially formed," while "neither Hsu nor

Meyyappan [i.e., prior art] . . . define a window at the conductive layer which is smaller in at least one direction on the auxiliary window initially formed in the first dielectric layer." Ex. F ('336 FH) at INV-SAM-753-54. Thus, because only Samsung's construction is true to the '336 Patent's object and claimed method for achieving that object, it should be adopted.

2. "continuing etching" means "without interruption, to go on etching"

The specification discloses that after the prior step of "etching the additional dielectric layer back anisotropically" ends, the "contin[ued] etching anisotropically" step begins without interruption. Specifically, it describes the first "etching" step as removing an oxide layer 9 by "anisotropic etching-back" to form "spacers . . . on the side walls of the auxiliary windows 8." '336, 3:62-4:1. The specification then describes the "continuing etching" step by stating: "***The etching treatment is continued*** . . ." to etch the "oxide layer 5." *Id*., 4:1-3 (emphasis added). The definite article "The" signals that the "etching treatment" refers to the same "etching-back" described earlier. Fair Decl. ¶¶80-81. Thus, in Claim 1, the final "continuing etching" step is simply a continuation of the same anisotropic "etching" process in the prior step. *Id*.

At no point does the specification disclose two separate and distinct etching processes with an interruption in between. Indeed, to interrupt the etching between the etching of oxide layer 9 and continued etching of oxide layer 5, as Invensas proposes, would require the etch process to stop needlessly midway through the process. *Id*., ¶¶82-83. But such an interrupted etch process contradicts the claim's recitation of a "continued" etching process and is neither supported nor enabled by the intrinsic record. It would also add complexity and slow manufacturing. *Id*.

Invensas provides no basis for finding that there is an interruption between the "etching" and "continued etching" steps. It instead misreads the patent's statement that "etching treatment may be simply stopped the moment the poly layer 3 [the conductive layer] is reached" as evidence that the "continued etching" follows an interruption. D.I. 123, 21 (citing '336, 4:8-10). The

"stopped" language relates to Figure 1f and when the last "continuing etching" step can ***conclude*** after it has already been in progress. Fair Decl. ¶¶84-85. By contrast, Samsung's construction, as supported by Figures 1d to 1e and related text at 4:1-8, concerns when the "continuing etching" step ***begins***. Under the construction, the "continuing etching" step begins without interruption after the prior "etching" step ends. Invensas's cited specification text does not address the transition between the "etching" and "continuing etching" steps, and is therefore irrelevant.

Invensas also cites dictionaries defining "continuing" as coming "after an interruption." At best, its dictionaries conflict with other dictionaries defining "continue" as "to maintain without interruption a condition, course, or action." Ex. G, SAMSUNG-INVENSAS-113146 (p. 251); Ex. H, SAMSUNG-INVENSAS-113128 (p. 408). Given the conflicting extrinsic definitions, the construction should be resolved from the intrinsic evidence. Here, the intrinsic evidence dictates that "continuing etching" must follow the prior "etching" step without interruption.

C. "providing a first dielectric layer adjacent the substrate"

Plaintiff's Proposal	Defendants' Proposal
Plain and ordinary meaning, no construction necessary. Alternatively: "providing a first dielectric layer near the substrate"	Plain and ordinary meaning, no construction necessary.

Although the parties agree that no construction is required, Invensas nonetheless advocates for its alternative construction based on speculation that Samsung intends to later argue non-infringement based on its original proposal that "adjacent" means "without intervening layers." D.I. 123, 22-23. Samsung has no such intention. Samsung nonetheless opposes Invensas's attempt to replace the word "adjacent" with "near," a word that is meaningless in the context of the '336 Patent and renders the claims indefinite. *E.g.*, *In re Neurografix ('360) Patent Litig.*, 201 F. Supp. 3d 206, 222-23 (D. Mass. 2016) (finding term with "near" indefinite). As the specification describes, the layers formed according to Claim 1's method are all less than a micrometer in thickness. '336, 3:30-43 (describing thicknesses of "0.1 μm," "60nm," "0.5 μm"). Neither the

specification nor Invensas's construction provides any objective boundaries on what constitutes "near" given these microscopic dimensions. Fair Decl. ¶¶87-88. And if the jury were to adopt a lay understanding of "near," this would render "adjacent" meaningless because any layer is only micrometers away from the substrate. *Id*.; *see Curtiss-Wright Flow Control Corp. v. Velan, Inc*., 438 F.3d 1374, 1379 (Fed. Cir. 2006) (rejecting district court's construction of "adjustable" as rendering the term meaningless because "it [is] difficult, if not impossible, to imagine any mechanical device that is not 'adjustable' under the district court's construction").

III. U.S. PATENT NOS. 6,566,167 (CLAIMS 1-12) AND 6,825,554 (CLAIMS 1-5)

A. "to isolate…" / "to create…" / "to provide…" Terms

Term	Plaintiff's Proposal	Defendants' Proposal
"to isolate the signal traces and thereby provide noise shielding" ('167, Cl. 1, 11)	Plain meaning, no intent required	"for the purpose of providing a shield between the signal traces in order to reduce electrical noise"
"to isolate the two groups of signals" ('167, Cl. 6, 12)	Plain meaning, no intent required	"for the purpose of providing a shield between two groups of signals"
"to create a bottom-layer isolating ground trace" ('167, Cl., 1, 6, 11, 12)	Plain meaning, no intent required	"for the purpose of creating a bottom-layer isolating ground trace"
"to create a second-layer isolating ground trace" ('554, Cl. 1)	Plain meaning, no intent required	"for the purpose of creating a second-layer isolating ground trace"
"to provide noise shielding" ('554, Cl. 1)	Plain meaning, no intent required	"in order to provide a shield that reduces electrical noise"

For these five terms, Samsung proposes the same constructions that the District of Delaware adopted for these same terms in the '167 and '554 Patents in an action filed by Invensas. *Invensas Corp. v. Renesas Elecs. Corp.,* No. 11-448-GMS, 2013 WL 3753621, at *2 nn.10-12, 16-17 (D. Del. July 15, 2013) ("*Renesas* Order"). This Court has routinely adopted prior constructions of other courts, reasoning that "prior claim construction proceedings involving the same patents-in-suit are 'entitled to reasoned deference under the broad principals of stare decisis and the goals articulated by the Supreme Court in *Markman*.'" *E.g.*, *Mobile Telecomms. Techs., LLC v. ZTE (USA) Inc.*, No. 2:13-CV-946-JRG-RSP, 2016 WL 1435603, at *3 (E.D. Tex. Apr. 12, 2016).

Invensas seeks a second bite at the apple by re-litigating these constructions. Indeed, Invensas repeats its failed arguments from *Renesas*—namely, that it is improper to include a purpose requirement in claims because "patent infringement is a strict liability tort" and that the disputed terms recite an "effect" or "result," not a purpose. *Compare* D.I. 123, 28-30, *with* Ex. I, 14-17 and Ex. J, 8-12 (Invensas's briefs in *Renesas*). The Delaware court properly rejected these very arguments, finding instead that including a purpose requirement is appropriate where, as here, it is compelled by the intrinsic record. *Renesas* Order, at *2 nn.10-12, 16-17.

As an initial matter, there is no prohibition against construing a claim to require purpose or intent. In *Jansen v. Rexall Sundown, Inc.*, the claims recited a method "for treating or preventing macrocytic-megaloblastic anemia" to be applied to "a human in need thereof." 342 F.3d 1329, 1330, 1332 (Fed. Cir. 2003). The Federal Circuit found that these claims included a "statement of the ***intentional purpose*** for which the method must be performed," and performing the claim steps "for some purpose other than treating or preventing macrocytic-megaloblastic anemia is not practicing the claimed method." *Id*. at 1333-34 (emphasis added). In *Paragon Solutions, LLC v. Timex Corp*., the Federal Circuit construed the term "displaying real time data" as "displaying data without ***intentional delay*** . . ." because "the specification supports a construction of 'real-time' in this case that precludes intentionally delaying the display of data by storing it for later review." 566 F.3d 1075, 1089, 1092-93 (Fed. Cir. 2009) (emphasis added). And in *3M Co. v. Avery Dennison Corp.*, a court categorically rejected the notion that only method claims can include an "intent requirement," stating "there is no binding authority for the position that an apparatus claim may not include an intent element." No. 10–2630 (MJD/FLN), 2013 WL 673838, at *3 (D. Minn. Feb. 25, 2013). This District has also routinely adopted purpose or intent requirements:

- *Parthenon Unified Memory Architecture, LLC v. HTC Corp.*, No. 2:14-CV-00691-JRG-RSP, 2015 WL 4594583, at *19 (E.D. Tex. July 30, 2015): This Court construed "directly supplied" to mean "supplied without being stored in main memory ***for purposes of*** decoding subsequent images."

- *PACT XPP Techs., AG v. Xilinx, Inc*., No. 2:07-CV-563-CE, 2011 WL 2469909, at *28 (E.D. Tex. June 17, 2011): The court construed "configuration unit" as "unit for configuring and reconfiguring a PAE or logic cell. Embodied by a microcontroller specifically designed ***for this purpose***."

- *Wi-Lan Inc. v. Acer, Inc.*, No. 2:07-CV-473-TJW, 2010 WL 3766551, at *17 (E.D. Tex. Sept. 20, 2010): The court construed "shut-down condition" as "an express signal used ***for the purposes*** of entering a low-power state or a loss of framing."

- *Alcatel USA Sourcing, Inc. v. Microsoft Corp.*, No. 6:06-CV-499, 2008 WL 3914889, at *6 (E.D. Tex. Aug. 21, 2008): The court construed "MAC-based authentication flow" as "information exchange in which the authentication client uses the MAC address of the authentication agent ***for the purposes of*** authentication."

Here, as the *Renesas* Order found, including a purpose requirement is necessary because each of the five disputed terms includes a "to" clause that signals a purpose. *Renesas* Order, at *2 n.10. For example, the '554 Patent, Claim 1 recites "at least one isolating ground trace on the first layer between two signal traces ***to provide noise shielding***; and an array of solder balls on a second layer such that at least one row of solder balls is connected together and to ground ***to create a second-layer isolating ground trace***." The '167 Patent, Claim 1 similarly recites: "(d) patterning a grounded isolation trace adjacent to one of the groups of traces ***to isolate the signal traces and thereby provide noise shielding***; . . . (f) connecting the row of solder balls together and to ground ***to create a bottom-layer isolating ground trace***." *See also* '167, Claims 6, 11, 12. The *Renesas* Order reasoned: "the word 'to' is consistent with an intent requirement—in ordinary usage, it functions as a synonym for phrases like 'in order to' or 'for the purpose of.'" *Renesas* Order, *2 n.10. The *Renesas* Order cited *Whirlpool Corp. v. LG Electronics, Inc.*, where a court found "***to*** cool said fabric" constituted a "purpose clause" in the phrase "prior to draining said lesser concentrated detergent solution from said wash chamber, fresh water is added ***to*** cool said fabric." 423 F. Supp. 2d 730, 753 (W.D. Mich. 2004) (emphasis added). Similar words, such as "for," have also been construed as requiring a purpose. *Rapoport v. Dement*, 254 F.3d 1053, 1061 (Fed. Cir. 2001) (construing a method "***for*** treatment of sleep apnea" as requiring that the method be

performed "***with the intent*** to cure the underlying condition" of sleep apnea); *S. Snow Mfg. Co. v. Snowizard Holdings, Inc.*, No. CV 06-9170, 2013 WL 12229039, at *7 (E.D. La. Jan. 2, 2013) (construing "the second end has formed in a bottom surface thereof, a[n] indented cavity ***for*** receipt of a ratchet tooth" as "the bottom surface at the end of the arm of the cam has a hollowed-out space set in from the margin ***for the purpose*** of receiving a ratchet tooth").

Against these many authorities, Invensas cites a 25-year old decision, *Texas Instruments Inc. v. U.S. Int'l Trade Comm'n*, 988 F.2d 1165 (Fed. Cir. 1993). But reliance on *Texas Instruments* is misplaced because it did not address whether purpose or intent could be a limitation or adopted as part of a construction. Instead, it addressed whether claim language "relating to the velocity of the fluid inside the mold" should be given any "weight in [the] infringement analysis" when it followed the terms "whereby" or "to." *Id*. at 1172. In deciding no weight was entitled, the Federal Circuit stated that "a 'whereby' clause that merely states the result of the limitations in the claim adds nothing to the patentability or substance of the claim." *Id*. The court reached the same conclusion for the "to" clause because it recited the same velocity-related result as the "whereby" clause. *Id*. Thus, *Texas Instruments* addresses only whether a claimed result can be limiting — not whether a purpose can be limiting or part of a construction. Moreover, *Texas Instruments* is distinguishable because the claimed result relating to "velocity of the fluid inside the mold" was not the purpose of the patent at issue. *See* Ex. K. In contrast, the '167 and '554 Patents repeatedly describe noise shielding and isolation as fundamental to the alleged invention:

- Title: "PBGA electrical ***noise isolation*** of signal traces"
- Abstract: "According to the present invention, a grounded isolation trace is then patterned adjacent to one of the groups of traces ***to isolate the signal traces, thereby providing noise shielding***."
- Field of Invention (1:7-10): "The present invention relates to ball grid array type semiconductor packages, and more particularly to the design of a trace layout ***to isolate electrical noise*** between two adjacent sets of signals in a 2-layer PBGA substrate."

- Background (1:53-56): "Accordingly, what is needed [is] a method for fabricating a semiconductor package ***to reduce electrical noise*** between adjacent signals in a 2-layer PBGA without adding additional layers. The present invention addresses such a need."

- Summary of Invention (1:64-67): "According to the present invention, a grounded isolation trace is then patterned adjacent to one of the groups of traces ***to isolate the signal traces, thereby providing noise shielding***."

The inventors affirmed the centrality of purpose to the claims, explaining that limitations such as an "isolating ground trace" must by definition serve the purpose of isolation. First-named inventor, Wee Liew, who drafted much of the specification and claims, confirmed that "what makes an isolating ground trace an isolating ground trace is whether the ***objective*** is to isolate signals." Ex. L, 35:25-38:14, 91:12-92:11 (emphasis added). He elaborated that if a ground trace's "objective is to isolate a certain set of signals, yeah, then we call isolating ground trace," but if a ground trace's "objective is not to isolate signals, that ground trace is not an isolating ground trace." *Id*., 90:20-92:5. The second inventor confirmed that a trace is "only called an isolation ground trace if you use it for the reason of isolating and [re]ducing noise," and if "you weren't using [a trace] for that reason, it's not an isolation ground trace anymore." Ex. M, 59:7-60:8.

In addition, while Invensas tries to distinguish *Jansen* on grounds that it adopted a purpose limitation because the patentee relied on it to distinguish prior art (D.I. 123, 30), Mr. Liew also relied on the patents' purpose requirement to distinguish prior art. When presented with prior art disclosing ground traces that had "the effect of reducing [] noise" between signal traces, Mr. Liew distinguished it because its ground traces' "main purpose . . . is not to reduce the noise of the adjacent signals." Ex. N, 91:16-92:20. Unlike the prior art, the '167 and '554 Patents' "ground traces are specifically for the purpose of reducing noise in adjacent signal traces." *Id*., 92:21-23. The inventors' testimony confirms that merely having the claimed features like a ground trace is insufficient to meet the claims, even if they have the "effect" of reducing noise. Instead, to meet the claims, the features must be used for the purpose of reducing noise and isolating signal traces.

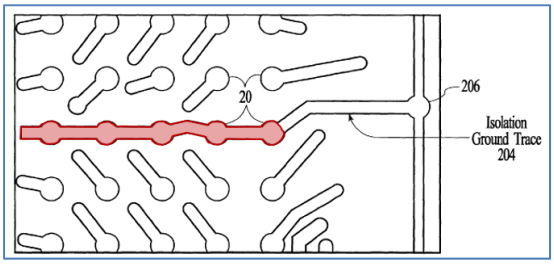
Thus, the claim language, specification, and inventor testimony all confirm the *Renesas* Order's finding that a "purpose" requirement is included in the claims.

B. "row of solder balls" ('167, Cl. 1, 6, 11, 12; '554, Cl. 1)

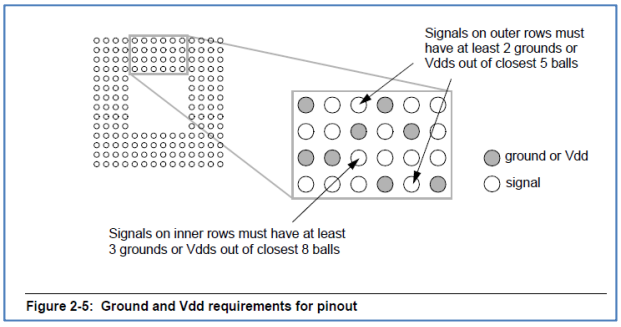
Plaintiff's Proposal	Defendants' Proposal
"three or more solder balls arranged next to each other in a line"	"three or more solder balls arranged next to each other in a horizontal or vertical line"

Invensas's proposal that the claimed "row" broadly encompasses solder balls arranged next to each other in any line — sweeping in circular, diagonal, zigzag, or triangular arrangements of solder balls — is unsupported by the intrinsic record and contrary to the term's ordinary meaning. Samsung's construction of a "horizontal or vertical line," by contrast, follows from the intrinsic evidence and the ordinary meaning of "row of solder balls" to those of ordinary skill.

First, Samsung's construction is supported by the specification. The "row of solder balls" recited in the claims corresponds to the "row of the solder balls 20" in the specification, which Figure 4 depicts as a horizontal line of five balls (in red), connected to via 206. '167, 3:12-21.



Second, it is supported by prior art cited during prosecution, which is part of the intrinsic record. *Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003). The Rambus "Package Selection Guide" cited during prosecution describes two "inner" and "outer" "rows" of solder balls in Figure 2-5, where each of the four total rows is a horizontal line. Ex. O, SAMSUNG-INVENSAS-112832 (p. 5).



Third, Samsung's construction is supported by the common usage of "row" in the art. Inventor Wee Liew testified that the patents' depiction of horizontal rows of solder balls reflected

an actual implementation that followed industry standards published by the Joint Electron Device Engineering Council (JEDEC). Ex. L, 59:21-60:24. As Mr. Liew explained, JEDEC standards "represent a common understanding of the industry" and "the terminology used in JEDEC standard represented the common use of those terms in the industry." *Id*., 31:20-32:25. JEDEC standards by 2001 all describe solder balls arranged in horizontal "rows." One standard describes a "6-row" ball matrix, which its Figure 1 depicts as six horizontal lines. Ex. P (JESD75), SAMSUNG-INVENSAS-112796-97.

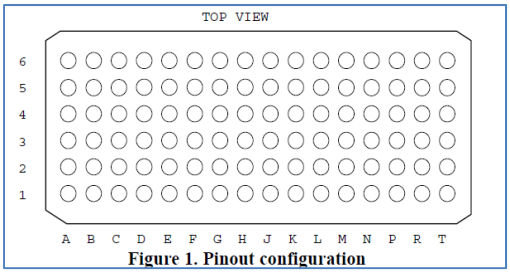


Figure 1. Pinout configuration

Invensas, on the other hand, cites nothing from the intrinsic record showing that a "row" can be any "line." It instead cites a non-technical definition of "row" and two unrelated patents, filed years after the '167 and '554 Patents, that use "row" in a specialized manner different from its use in the context of the '167 and '554 Patents and its common usage in the semiconductor field. D.I. 123, 25. Because Samsung's construction is supported by the intrinsic evidence and industry standards, whereas Invensas's proposal is not, Samsung's construction should be adopted.

C. "trace" ('167, Cl. 1-12; '554, Cl. 1-5)

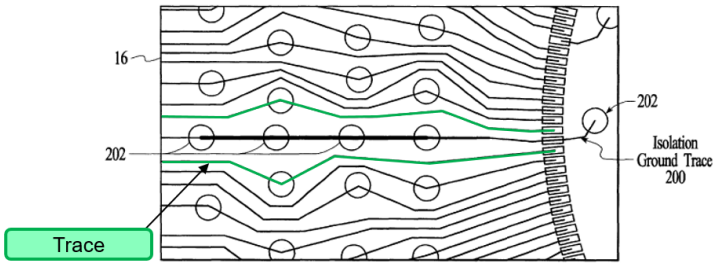
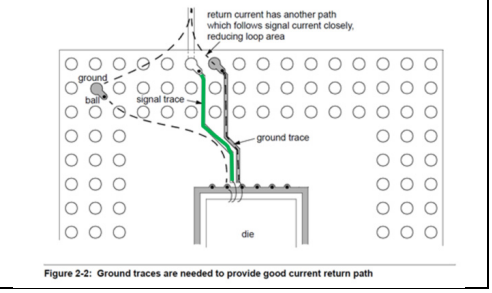
Plaintiff's Proposal	Defendants' Proposal
"conductive path on an insulating substrate"	"conductive line on an insulating substrate"

The parties' proposals for "trace" differ in only one word — "line" (in Samsung's proposal) versus "path" (in Invensas's proposal). Samsung's construction with "line" is taken straight from the specification in column 1, lines 12-18. By contrast, not once does the word "path" ever appear in the specification or file histories. Yet Invensas alleges Samsung's construction would somehow confuse the jury because a "line" implies a "straight line." D.I. 123, 26.[5] Not so.

The intrinsic evidence demonstrates that "trace" refers to a "line," not a "path." The

[5] To the extent the Court agrees that "line" may be misinterpreted as a "straight line," Samsung is amenable to clarification that the "line" need not be straight.

specification equates the word "trace" with "conductive line on an insulating substrate," stating: "Ball grid array (BGA) packages are constructed with die mounted on a substrate with . . . ***conductive lines or traces*** on the surface substrate." '167, 1:12-18 (emphasis added). This use of "or" connotes that "conductive line" and "trace" are synonymous. *See, e.g., PSN Ill., LLC v. Ivoclar Vivadent, Inc.*, No. 04 C 7232, 2006 WL 3523760, at *5 (N.D. Ill. Dec. 7, 2006) (finding the specification statement, "[a] ***model or statue*** of the tooth or teeth," meant that "model" was a "synonym" for "statue" in the claim (emphasis added)). Invensas's argument that "or" is disjunctive is refuted by the intrinsic evidence. Figure 3 below depicts all "traces" such as the two annotated in green, as conductive lines. And the Rambus Guide cited during prosecution depicts a "ground trace" and "signal trace" as lines. Ex. O, SAMSUNG-INVENSAS-112830.

'167, Figure 3 (annotated)	**Cited Art, Rambus Guide, Fig. 2-2 (annotated)**
	

Disregarding the intrinsic evidence, Invensas proposes defining a "trace" using the word "path" that it never identifies in the patents, file histories, or cited art. And Mr. Liew, who personally drew the figures and drafted the claims, affirmed that a trace "***doesn't refer to any path*** or pattern that happens to be conductive." Ex. L, 68:18-69:2 (emphasis added). Instead, a "trace" refers only to "conductive patterns which . . . have a thin linear shape." *Id*. He also confirmed that "in the context of [the '167 and '554] patent[s], conductive line and trace mean the same thing" and are "interchangeable" words. *Id*., 69:4-70:23. Thus, based on the specification, cited art, and inventor testimony, a "trace" refers to a "conductive ***line*** on an insulating substrate."

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on July 26, 2018.

/s/ Brian Berliner